

3



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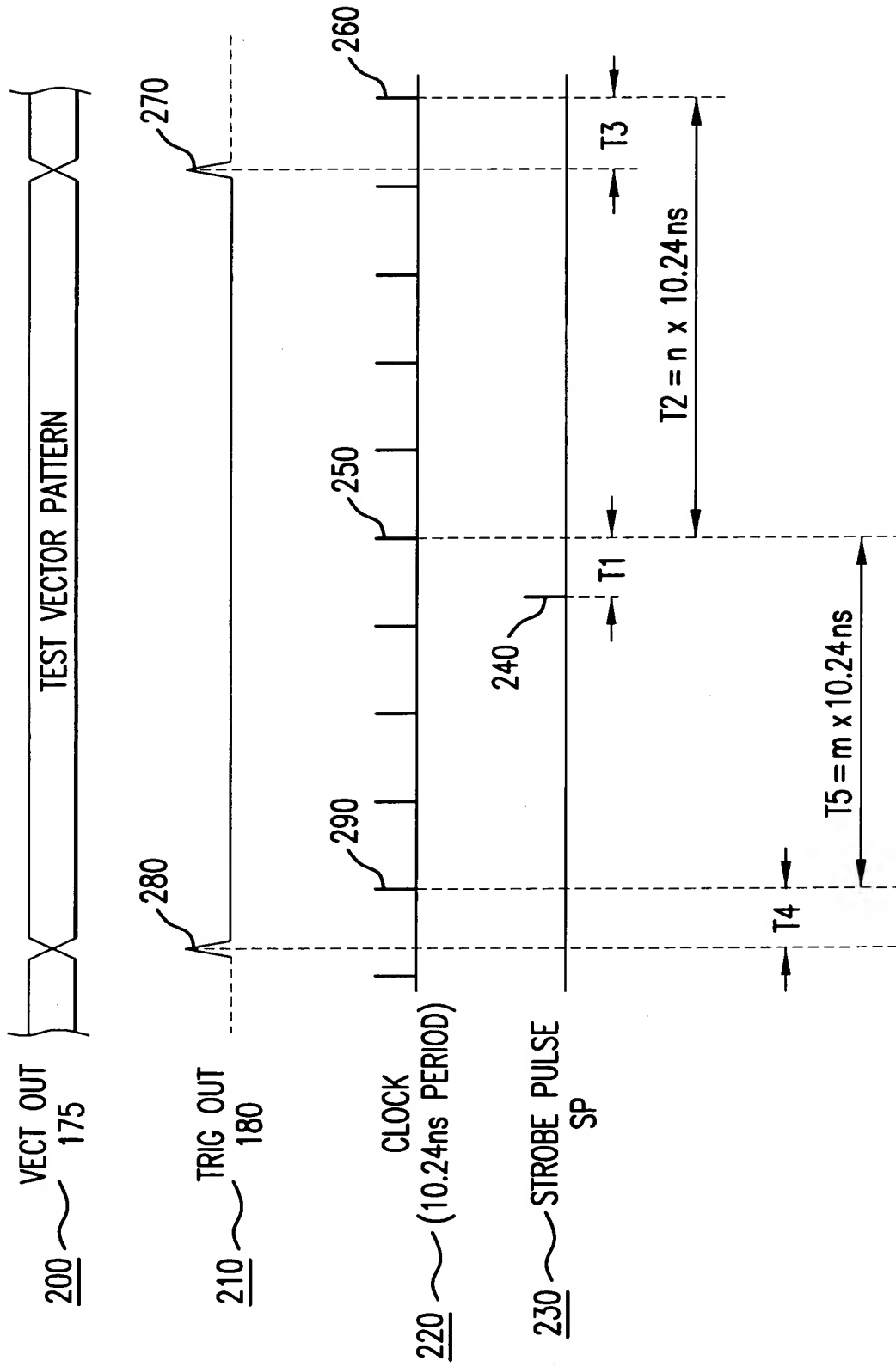


FIG. 2

FIG. 3

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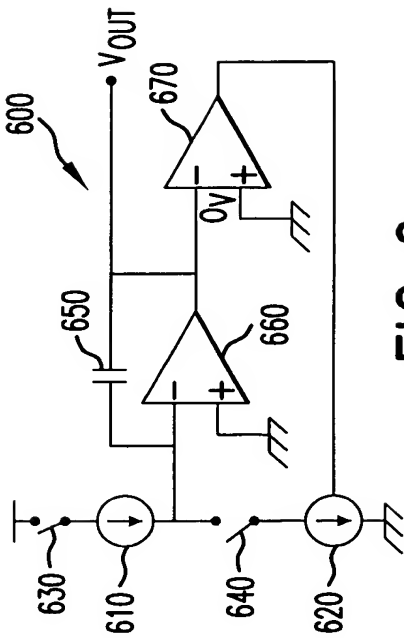


FIG. 6

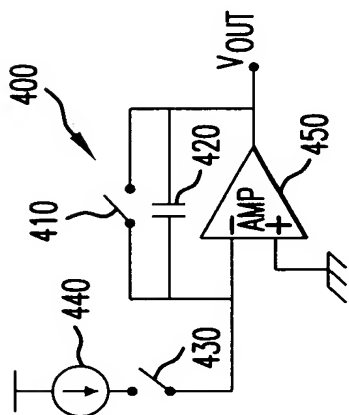


FIG. 4

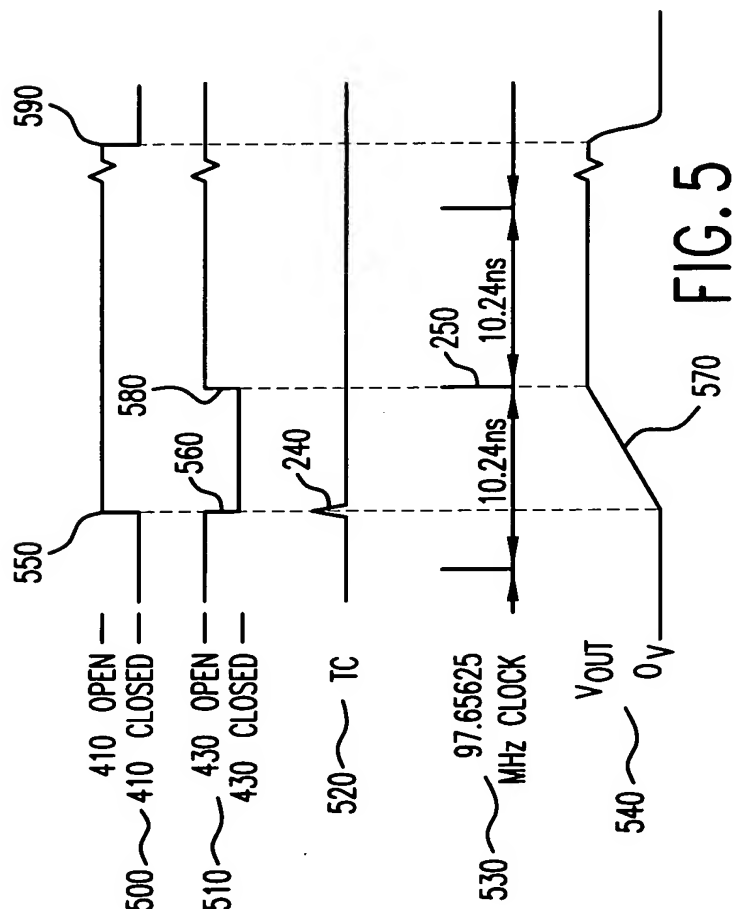


FIG. 5

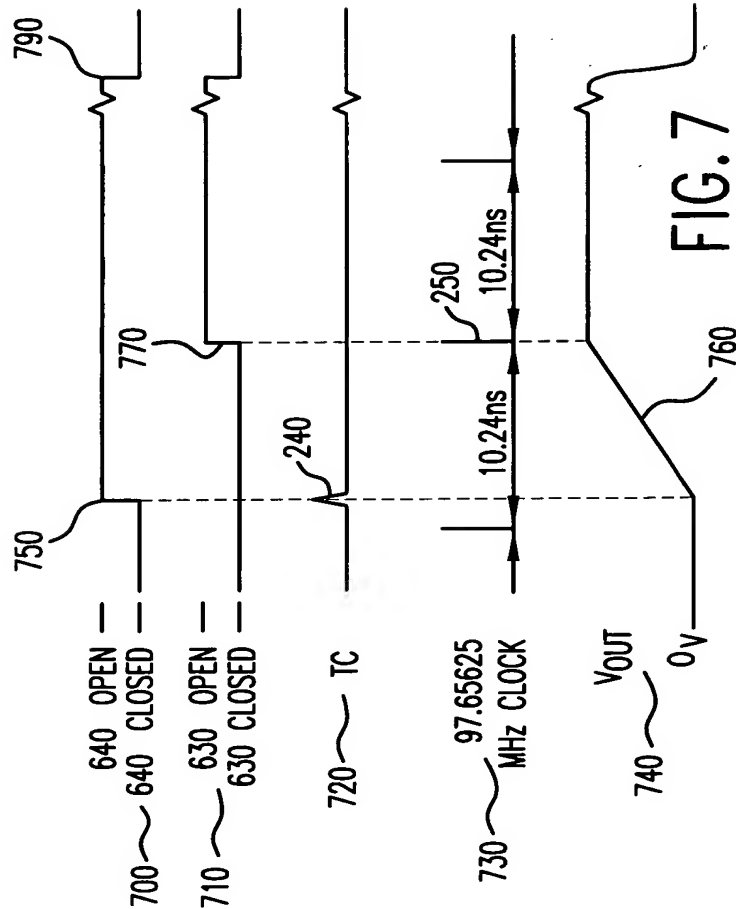
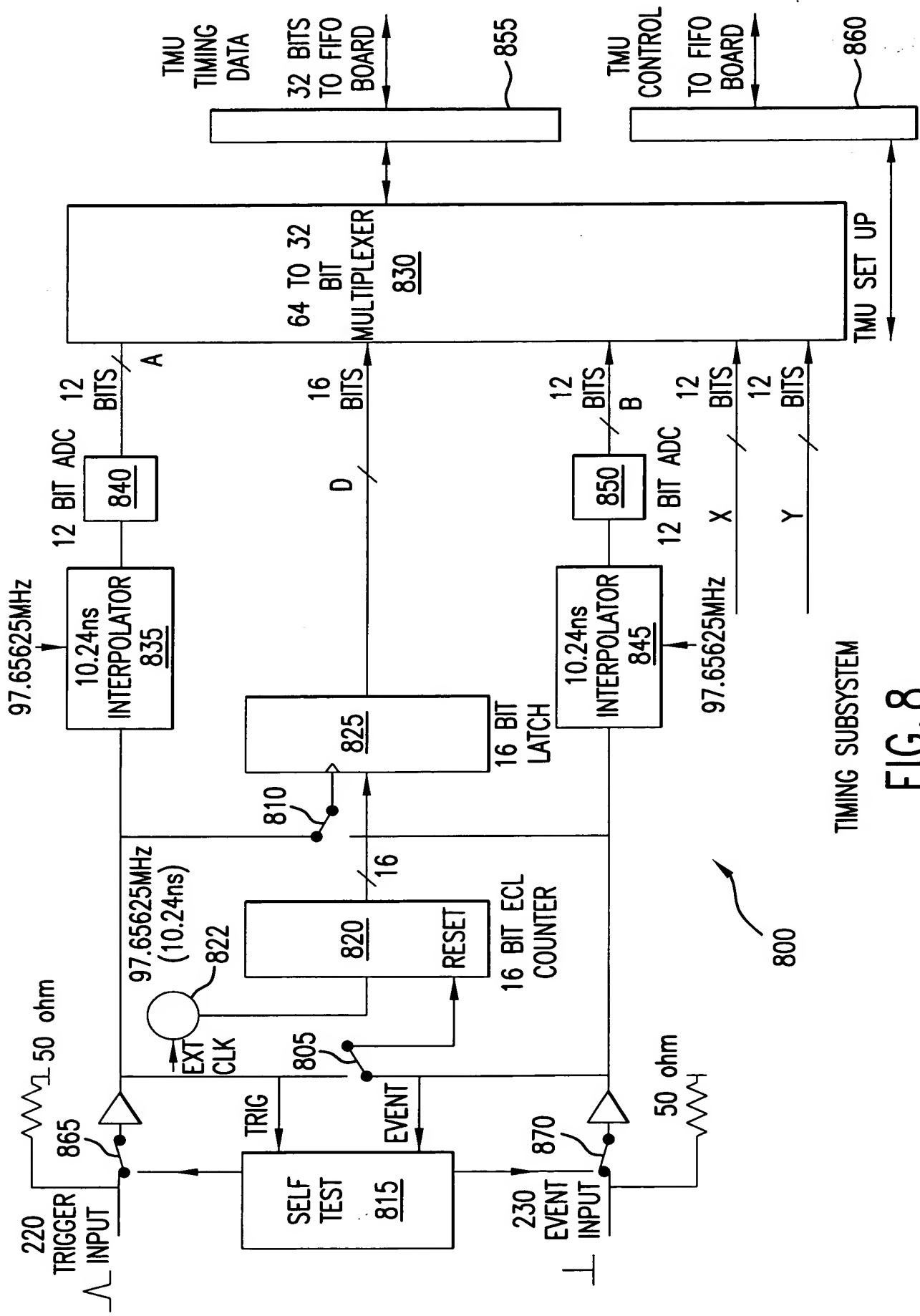


FIG. 7

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TIMING SUBSYSTEM

FIG. 8

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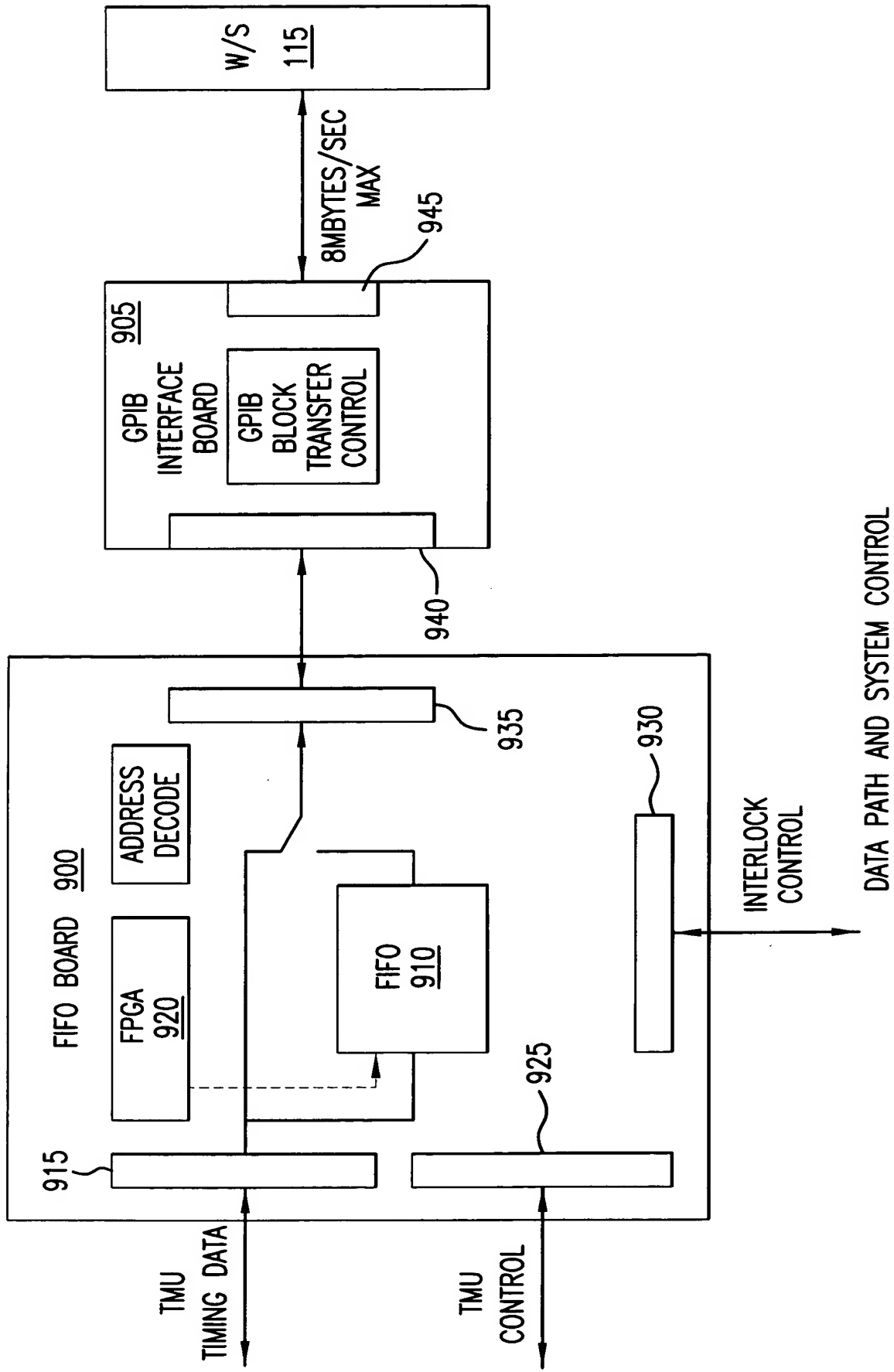


FIG. 9

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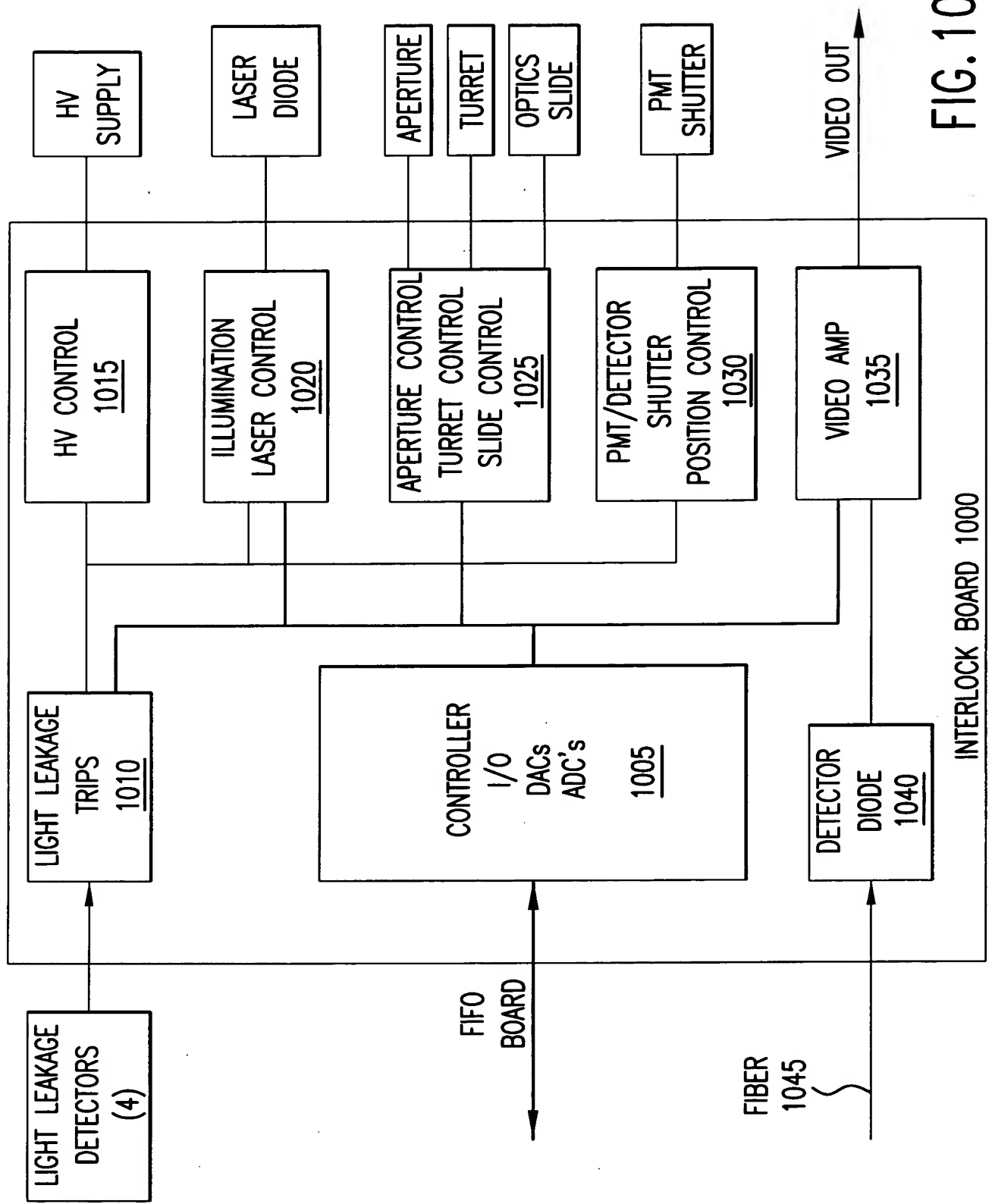


FIG. 10

The diagram illustrates a TMU clock generator (1100) with two parallel clock paths. The top path begins with a 100MHz VCXO (1135) and the bottom path with a 97.65625MHz VCO (1105). Both paths include dividers (1125, 125), phase comparators (1130, 1155), and further dividers (1140, 128) leading to XTAL (1150) and 100XTAL (1180) outputs. A self-test block (815) is also shown.

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INTERPOLATOR CALIBRATION METHOD

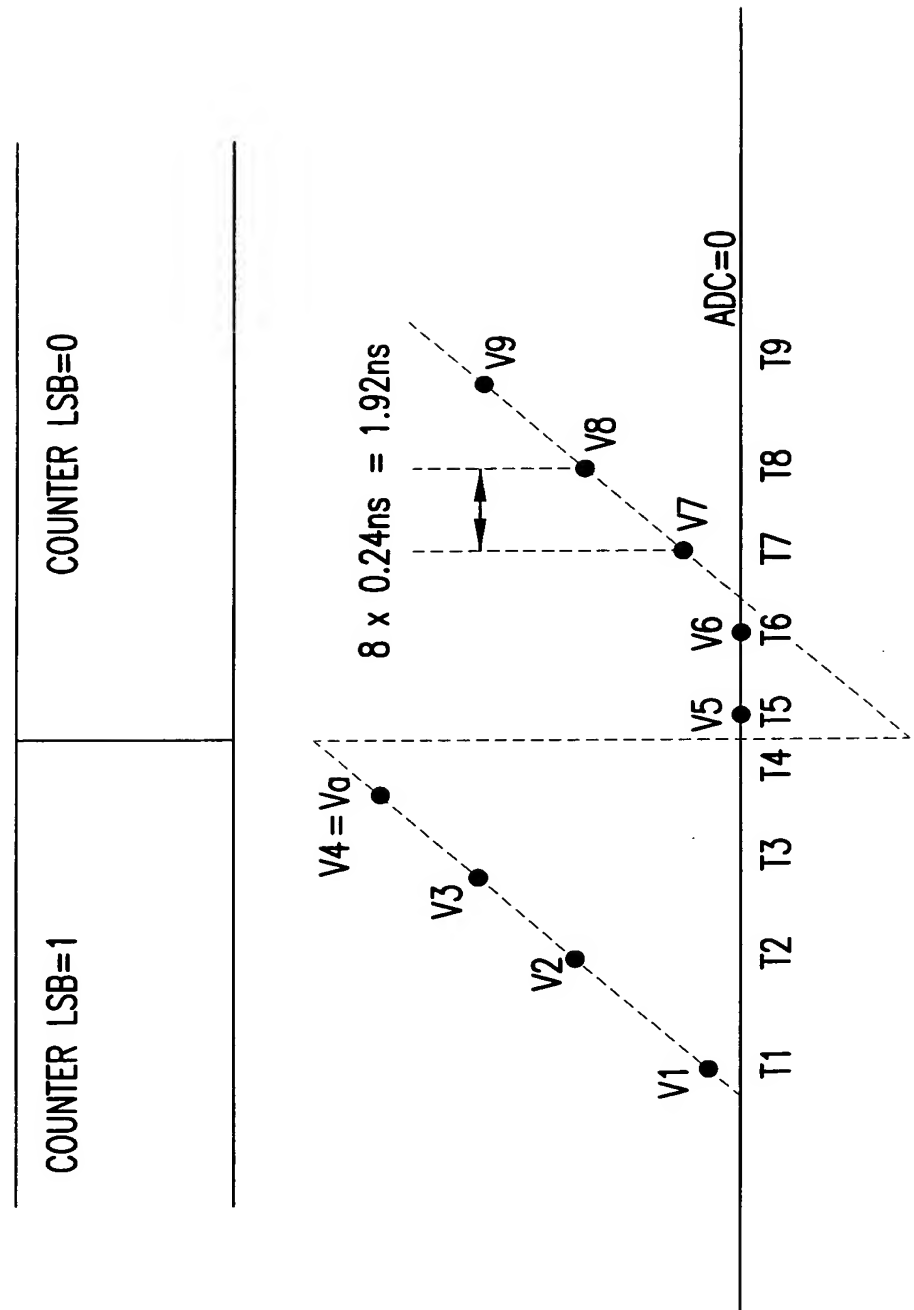


FIG.12

INTERPOLATOR CALIBRATION METHOD

COUNTER LSB=1	COUNTER LSB=0

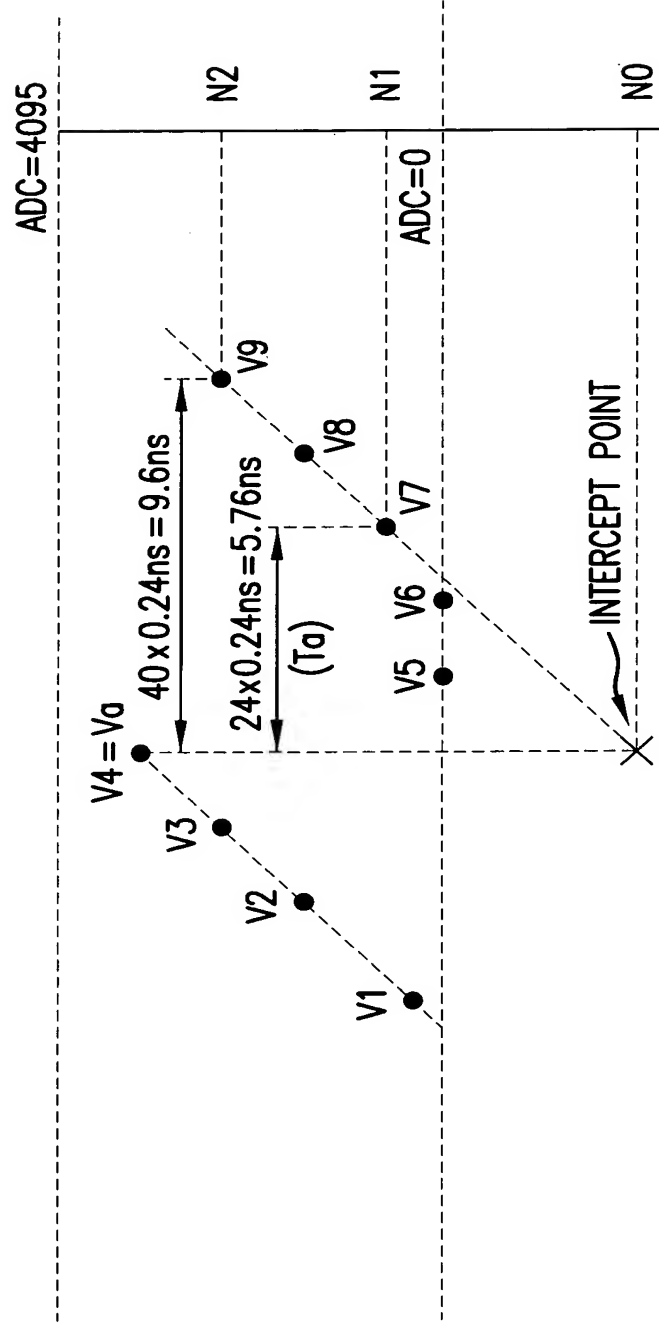


FIG.13

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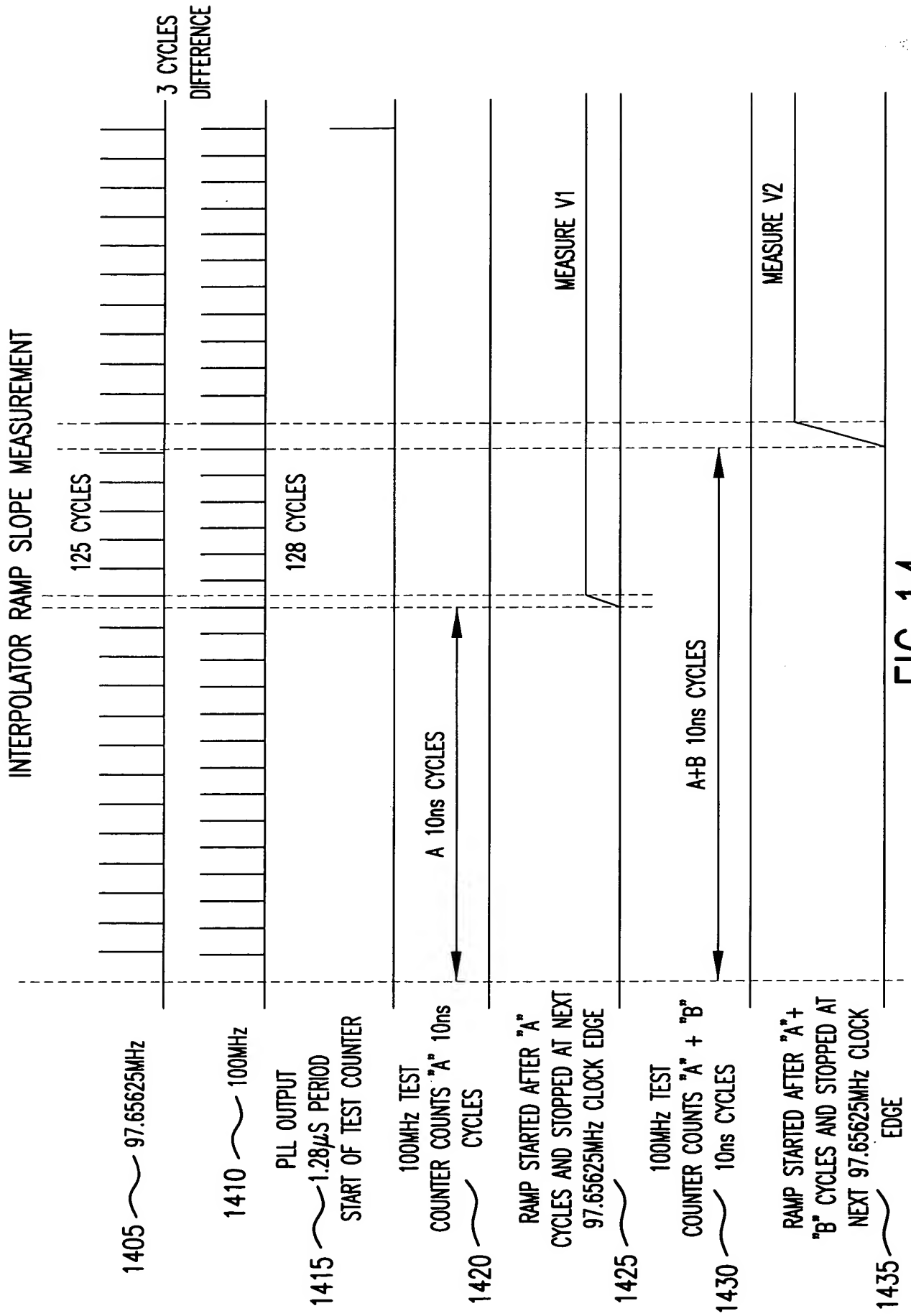


FIG. 14